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2.6 kV 4H-SiC Lateral DMOSFET's

J. Spitz, M. R. Melloch, *Senior Member, IEEE*, J. A. Cooper, Jr., and M. A. Capano

Abstract— **A 4H-SiC lateral double-implanted metal-oxide-semiconductor (LDMOS) field effect transistor is fabricated in a lightly doped n-epilayer on an insulating 4H-SiC substrate. After depleting through the epilayer, the depletion region continues to move laterally toward the drain. The result is an increase in blocking voltage compared to a vertical DMOSFET fabricated in the same epilayer on a conducting substrate. A blocking voltage of 2.6 kV is obtained, nearly double the highest previously demonstrated blocking voltage for a SiC MOSFET.**

I. Introduction

THE high avalanche breakdown field (2–3 MV/cm) of SiC makes it an attractive material for high-voltage, high-power devices [1]. SiC can also be thermally oxidized to form device quality SiO_2/SiC interfaces [2]. This makes it possible to fabricate a variety of MOS-based power switching devices in SiC. To date, all power MOSFET's demonstrated in SiC have been vertical structures such as UMOSFET's and DMOSFET's [3]–[6]. However, the blocking voltage of SiC DMOSFET's and UMOSFET's is theoretically limited to around 2 kV by the thickness of currently available SiC epilayers (about 10–15 μm). This limitation can be circumvented by constructing a lateral MOSFET on an insulating SiC substrate. In such a structure, the depletion region surrounding the p-well first depletes through the n-type epilayer to the insulating substrate, then moves laterally toward the drain. The lateral extent of the depletion region is therefore not limited by the thickness of the epilayer. Lateral power MOSFET's were first proposed by Appels and Vaes [7] in 1979, and have been the subject of renewed interest in the silicon power device community in the last several years [8]. In this letter we report the first LDMOS power FET in SiC. This device exhibits a blocking voltage of 2.6 kV, nearly double the highest previously demonstrated blocking voltage for any SiC power switching device.

II. Fabrication

The LDMOS structure shown in Fig. 1 consists of an insulating 4H-SiC substrate with a 15-μm epilayer doped n-type to 5×10^{14} cm^{-3}. A p-well is formed by implanting boron to a depth of 0.9 μm and annealing at 1600 °C for 40 min in Ar. The boron p-well is a retrograde implant profile at energies of 30, 50, 100, 160, 240, and 360 keV with doses of 1.5, 2.0, 3.0, 8.0, 28, and 36×10^{13} cm^{-2}, respectively. The n$^+$ source and drain regions are formed by implanting nitrogen and annealing uncapped at 1200 °C for 5 min in Ar [9]. A multiple nitrogen implant profile at energies of 30, 70, 120, and 190 keV with doses of 4.0, 6.5, 8.0, and 11×10^{14} cm^{-2}, respectively, is used. A 50-nm gate oxide is thermally grown at 1150 °C in wet O_2 [2], followed by deposition of polysilicon for the gate electrodes. The polysilicon is doped using a spin-on dopant, and gates are defined using reactive ion etching. The source and drain contacts are Ni, and the p-well contacts are Al. The contacts are not alloyed in these prototype devices. The p-well wraps around the periphery of the gate to form a guard ring that reduces the electric field in the oxide at the edges of the gate. Devices are fabricated with drain-to-guard-ring spacings up to 50 μm.

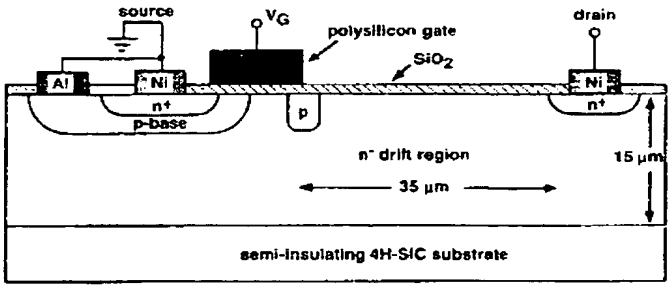

Fig. 1. Cross section of the 4H-SiC LDMOS power transistor.

III. Experimental Results

Fig. 2 shows the current–voltage ($I-V$) characteristic for an LDMOS device with 35-μm drain-to-guard-ring spacing, 10-μm channel length, and 130-μm channel width. The $I-V$ characteristic is measured with the device submerged in Fluorinert. The threshold voltage is 6 V, and the drain-to-source blocking voltage is 2.6 kV. The off-state leakage current ($V_G = 0$) is less than 10 nA out to the blocking voltage. Since the breakdown field of Fluorinert is lower than that of SiC, the blocking voltage is limited by the breakdown of the Fluorinert and not by the device. Depositing a thick, high-breakdown-field dielectric such as SiO_2 should increase the blocking voltage. If the blocking voltage were limited by the SiC, for our epilayer doping and a 35-μm drain-to-guard-ring spacing, a blocking voltage of about 4.5 kV would be expected.

Fig. 3 shows $I-V$ characteristics for small drain-to-source biases at temperatures of 23 °C and 155 °C. As seen in Fig. 3(a), the source and drain contacts are not ohmic at room temperature. Although a previous study [9] showed that nitrogen implants in 6H-SiC can be activated by a 1200 °C, 5 min Ar anneal, the same anneal conditions do not produce

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J. Spitz, M. R. Melloch, and J. A. Cooper, Jr. are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907-1285 USA.

M. A. Capano is with the Materials Directorate Wright Laboratory, Wright-Patterson AFB, OH 45433-7707 USA.

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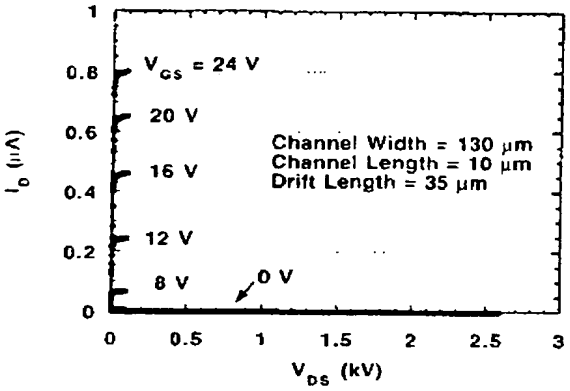

Fig. 2. Current–voltage characteristic of an LDMOS transistor with a 35-μm gate-to-drain spacing, measured at room temperature.

a high degree of activation in 4H-SiC. This is reflected in the poor ohmic contacts to our source and drain regions in these devices. This problem can be corrected by annealing at higher temperatures, such as 1500 °C.

The source and drain series resistance, along with a low inversion channel mobility, are the major factors limiting the on-current in these devices. The inversion channel mobility is estimated to be $7.5(\pm 2.5) \times 10^{-3}$ cm^2/Vs at room temperature, resulting in a specific on-resistance of about 550 Ω-cm^2. The I–V curves exhibit a 4 V offset near $V_{DS} = 0$, which we attribute to the nonohmic source and drain contacts. The inversion layer mobility increases by a factor of four in going from 23 to 155 °C. This thermally activated mobility has been reported by others [10], and is associated with defects at the SiO_2/SiC interface. In separate processing runs, we fabricated MOSFET's for measuring inversion layer mobilities on both 6H and 4H-SiC. Typical room temperature inversion layer mobilities in these devices are 35–50 cm^2/Vs on 6H-SiC and 4–5 cm2/Vs on 4H-SiC. The highest anneal temperature used in fabricating these mobility MOSFET's is 1200 °C. However, the LDMOS devices are exposed to a 1600 °C, 40-min anneal to activate the p-well implants. We believe that the 1600 °C anneal prior to gate oxidation causes surface roughening and step bunching [11] that degrades the inversion channel mobilities of completed LDMOS transistors. Similar mobility degradation is observed in mobility test devices on both 4H- and 6H-substrates that are annealed at 1600 °C, so this effect is clearly not related to the LDMOS structure. More work is needed to properly passivate the SiC surface during this 1600 °C activation anneal. We also typically observe lower inversion channel mobility as the epilayer thickness increases, which we attribute to increased step bunching with thicker epilayers. These steps may result in discontinuities in the inversion layer and an apparent low inversion layer mobility. Our LDMOSFET's are fabricated on very thick (15 μm) epilayers.

The specific on-resistance of the drift region in these devices is estimated to be about 200 mΩ-cm^2 for a 35-μm gate-to-drain spacing. This on-resistance can be reduced an order-of-magnitude by employing RESURF design principles [7], [12], [13]. In fact, the specific on-resistance of lateral devices

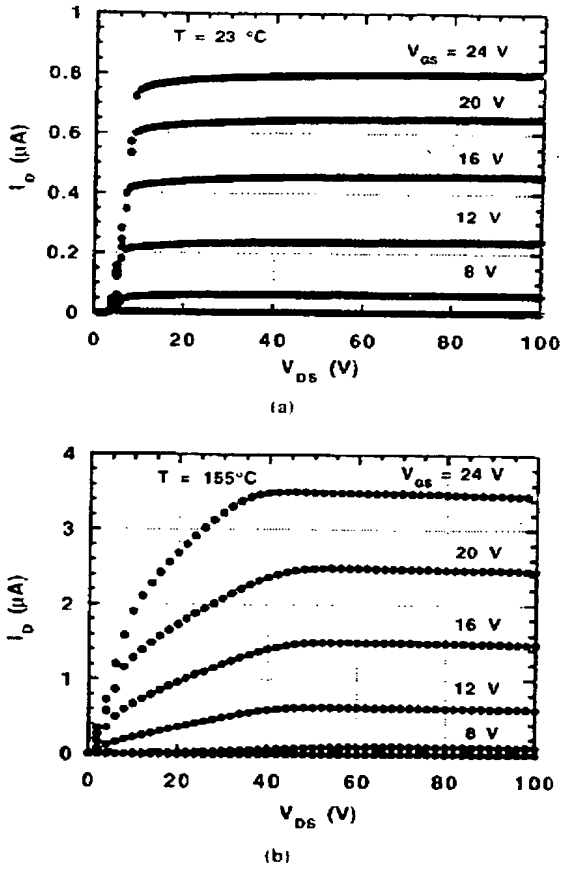

Fig. 3. Current–voltage characteristic of an LDMOS transistor at low drain-to-source biases at 23 °C and 155 °C. For these devices, the guard-ring-to-drain spacing is 35 μm, guard ring width is 15 μm, p-well-to-guard-ring spacing is 10 μm, channel length is 10 μm, and channel width is 130 μm.

designed with the reduced-surface-field (RESURF) principle can be up to four times lower than that of a comparable vertical device [12]. For this reason, lateral power MOSFET's are attractive alternatives to vertical MOSFET's for high-voltage applications.

IV. Summary

We have shown that a lateral DMOS transistor fabricated on an insulating SiC substrate can block extremely high drain voltages without the need for a thick epilayer. Under reverse bias, the depletion region surrounding the p-well first punches through to the insulating SiC substrate, then continues moving laterally toward the drain. The lateral extent of the depletion region is therefore not limited by the epilayer thickness. The present devices exhibit a blocking voltage of 2.6 kV, nearly double the highest previously reported blocking voltage for a SiC MOSFET.

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